COLECO INDUSTRIAL PARK
ASYLUM AVE., HARTFORD, CONN. 06105

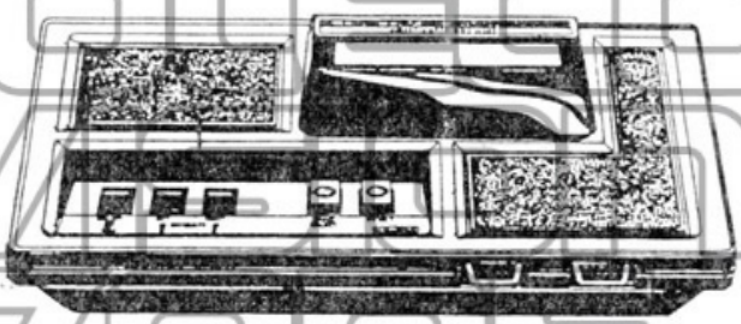
ENGINEERING PERFORMANCE SPECIFICATION # 194

REVISION B

ISSUE DATE 1-6-83

SHEET 1 OF 35

TITLE: ColecoVision Expansion Module #1 Model 2405



DISTRIBUTION:

F. Hickey
J. Mallardi
D. Zampini
M. Yoseloff
B. Hoskinson
J. Guberski
G. Vazac
C. Cheng
R. Goldstein
B. Crumnon
E. Bromley
R. Schenck
A. Bagley
Simmons - TW

	WRITTEN	PROJ. ENG.	ENG. APP.	MFG. APP.	
BY	C. Cheng	C. Cheng			
DATE	1-6-83	1-6-83	1-21-83		

REVISION LISTING

REVISION	PAGE	DATE	SECTION	ECO NO.	DESCRIPTION
A	1-35	1/6/83		V-10383	First Release
B	16	3/10/83	7.71	V-10459	Color Adjust Screen

1. Purpose

This specification establishes the performance specification and criteria for manufacturing the COLECOVISION Expansion Module #1 Model 2405 for American NTSC system.

2. Applicable Documents

#72019	Top Housing
#72020	Bottom Housing
#72029	Assembly
#91046	P.C. Board Assembly (Logic)
#91049	Schematic
#91657	Instruction Sheet
#92064	Final Test Cartridge
#92065	Color Test Cartridge
A20406	ColecoVision Specification/Bill of Materials
FCC ...	Part 15, Subpart J
QC 101	Coleco Toy and Game Standard
QC 102A	Transportation Test Procedure
QC 108	Sampling Specifications
QC 109	Handling and Operating Procedures for MOS Circuits
QC 111	Label and Graphic Standards
QC 114	P.C. Board Workmanship Standard

3. Acceptance

3.1 AQL (Acceptance Quality Level) of the finish console shall be:

1.0% AQL MAJOR

4.0% AQL MINOR

4. Environmental Requirements

At the completion of tests for following requirement, unit shall pass performance specification Item 7.

4.1 Operating Temperature Range: +10°C (50°F) to 40°C (104°F) at 70% RH.

4.2 Storage Temperature Range: -10°C (14°F) to 60°C (140°F) at 90% RH.

4.3 Thermal Shock: Shall withstand 10 cycles for one hour at each operating temperature extreme. Unit to stabilize for one hour at room temperature between temperature changes.

4.4 High Voltage Static Test: At all switches, housing openings, parting line, any metal surfaces withstand 25 KV discharge from a 200 pf capacitor with 10K ohms limiting resistor.

4.5 Vibration: Shall comply with standard per QC 102A.

4.6 Drop Test: Console shall withstand (3) 30" drops per QC 101. Shall comply with QC 102A (packaged).

5. Applicable Standards

5.1 Coleco Toy and Game Standard (QC 101 and CPSC).

5.2 Surface Coatings Standard, Label and Graphic Standards (QC 111 and CPSC).

6. Life

6.1 1000 hours minimum, shall be tested as follows: At 25°C ambient with connection to ColecoVision Console powered by COLECO POWER SUPPLY MODELS #55416 or #74942 (power switch in ON position) and a game cartridge is inserted into the unit under test.

6.2 Cartridge door assembly #78016 minimum 5000 openings tested to 90° of travel.

6.3 Cartridge connector #75465 minimum 5000 insertions @400-600 insertions/hour with contact resistance 0.5 ohms maximum. Contact resistance shall be determined with a virgin cartridge PCB before or after insertion test. Insertion test cartridge PCB must be less than 0.5 ohms contact resistance measured on a virgin cartridge connector.

6.4 Controller "D" connector #75450 minimum 1000 insertions/withdrawals (with cable). Maximum insertion force = 12 pounds. Minimum withdrawal force: 5 pounds. Maximum contact resistance = 0.5 ohms. Insertion/withdrawal force, contact resistance shall be determined with a virgin "D" connector. Insertion test "D" connector must be less than 0.5 ohms contact resistance and within force specification measured on a virgin male "D" connector.

6.5 Game select and reset switch #74933 minimum 10,000 operations with contact resistance not to exceed 200 ohms. Switch assembly including cap actuation force at center of cap to be 7± 2 oz.

6.6 Slide switch #74934 minimum 1000 operations with contact resistance not to exceed 0.03 ohms. Switch assembly including knobs actuation force both directions to be 21 ± 4 oz.

6.7 Expansion port edge connector minimum 1000 insertions/withdrawals. Maximum insertion force = 25 pounds and minimum withdrawal force = 5 pounds. Maximum contact resistance = 0.1 ohms. Shall be tested with a virgin PCB male edge connector only. PCB male test connector must be less than 0.1 ohms contact resistance and within force specification measured on a virgin female connector.

7. Performance Specification

7.1 General Test Conditions

7.11 A ColecoVision Console (EPS #183) powered by supply (EPS #190) is required for performing any test in this specification.

7.12 Ambient environment shall be 25^0C at 50% ±10% RH unless otherwise noted.

7.13 Module will be stablized to ambient condition before testing.

7.14 Two hand-controllers (EPS #184), switch box (R-74608), are required as accessories for performing some portion of the tests.

7.15 Test shall be performed only on color TV sets.

7.2 Power Supply Requirements

Three regulated DC voltages supplied by ColecoVision Console are required as below.

a. 5V +5%, -3% at 360 MA Max., 250 MA typical.

b. -5V ± 5% DC at 50 MA Max., 40 MA typical.

c. 12V ± 5% DC at 35 MA Max., 30 MA typical.

All DC voltages shall have no more than 10mV p-p ripple.

7.3 Radiation interference limits, line conducted interference limits shall meet FCC Part 15 specification on TV interface device under test condition Item 7.1, shall include two hand controllers connected to the module.

7.4 Clock Frequency

7.41 System Clock

System clock is supplied by ColecoVision Console and requirements are:

Main clock frequency shall be 3.579545 MHZ ± 125 HZ at U3 pin 26.

Rise and fall time to be max. 28 ns between 0.4 to 3.2V.

Logic high to be 112 to 168 ns at 4.0V.

Logic low to be 112 to 168 ns at 0.4V.

7.5 Current Drain

The individual currents drawn by the three DC voltages must not exceed limits as indicated in the power supply requirement item 7.2.

7.6 Composite Video Signal

7.61 The composite video signal shall meet American NTSC system and consist of following specification at Pin 33 of connector (Numbered per PCB layout) when using color test cartridge #92065.

Color	Chrominance AC Value (Volts)	Degree Related To Color Burst
White	–	–
Light Green	0.6	354
Medium Green	0.6	340
Dark Green	0.6	315
Light Blue	0.6	295
Medium Blue	0.6	270
Blue	0.6	237
Dark Blue	0.6	218
Light Purple	0.6	192
Purple	0.6	167
Light Red	0.6	147
Medium Red	0.6	115
Red	0.6	96
Dark Red	0.6	70
Light Brown	0.6	45
Green	0.6	25

Luminance Level (7)	DC Value (Volts)
Very High Luminance	0.77
High Luminance	0.65
Medium High Luminance	0.55
Medium Luminance	0.43
Medium Low Luminance	0.32
Low Luminance	0.21
Very Low Luminance	0.11

7.62 Timing Requirement

	PARAMETER	MIN	TYP	MAX	UNIT
tf1	Fall time, VBLACK to VSYNC		10		nS
tw(HS)	Pulse Width, Horizontal Sync		4.84		uS
tr1	Rise time, VSYNC to VBLACK		20		nS
tHS-CD	Delay time, Sync to Color Burst		372		nS
tw(CB)	Width, Color Burst		261		uS
tCB-LB	Delay time, Color Burst to left border		1.49		uS
tr2	Rise time, VBLACK to VWHITE		60		nS
tw(LB)	Left Border Video Width		2.42		uS
tf2	Fall time, VWHITE to VBLACK		110		nS
tw(AD)	Width of Active Display Area		47.68		uS
tw(RB)	Right Border Video Width		2.79		uS
tRB-HS	Delay time, Right Border to Horizontal Sync		1.49		uS
tVFB	Vertical Front Blanking		191.1		uS
tVS	Vertical Sync		191.1		uS
VVBB	Vertical Back Blanking		828		uS
tABA	Active plus Border Area Time		18.8		mS
	Number of color burst cycles		9		

7.63 Expansion Port (numbered per PCB layout) 60 pin total

Pin 1 Ground

Pin 2 Ground

Pin 11 Ground

Pin 13 Reset, Input - Table 7A, Timing Table 7B

Pin 31 Sound Output, Item 8.32

Pin 32 +12V

Pin 33 Composite vedio output, Item 7.61.

Pin 35 Ground

Pin 39 Ground

Pin 41 R/W Test Point

Pin 42 Ø2 Clock Test Point

Pin 45 Clock Input 3.58MHZ Item 7.61

Pin 57 +12V

Pin 58 +5V

Pin 59 +5V

Pin 60 -5V

Other pins are not used.

7.64 Cartridge Connector J1

Pin 1 A7 Output - Table 7A, Timing - Table 7B.

Pin 2 Ground

Pin 3 A6 Output - Table 7A, Timing - Table 7B.

Pin 4 VCC +5V, Item 7.2

Pin 5 A5 Output - Table 7A, Timing - Table 7B

Pin 6 A8 Output - Table 7A, Timing - Table 7B

Pin 7 A4 Output - Table 7A, Timing - Table 7B

Pin 8 A9 Output - Table 7A, Timing - Table 7B

Pin 9 A3 Output - Table 7A, Timing - Table 7B

Pin 10 A11 Output - Table 7A, Timing - Table 7B

Pin 11 A12 Output - Table 7A, Timing - Table 7B

Pin 12 A10 Output - Table 7A, Timing - Table 7B

Pin 13 A1 Output - Table 7A, Timing - Table 7B

Pin 14 CS Output - Table 7A, Timing - Table 7B

Pin 15 A2 Output - Table 7A, Timing - Table 7B

Pin 16 D7 Tri-State I/O - Table 7A, Timing - Table 7B

Pin 17 D0 Tri-State I/O - Table 7A, Timing - Table 7B

Pin 18 D6 Tri-State I/O - Table 7A, Timing - Table 7B

Pin 19 D1 Tri-State I/O - Table 7A, Timing - Table 7B

Pin 20 D5 Tri-State I/O - Table 7A, Timing - Table 7B

Pin 21 D2 Tri-State I/O - Table 7A, Timing - Table 7B

Pin 22 D4 Tri-State I/O - Table 7A, Timing - Table 7B

Pin 23 Ground

Pin 24 D3 Tri-State - I/O - Table 7A, Timing - Table 7B

Note = 1) X - Denotes active high

2) X - Denotes active low.

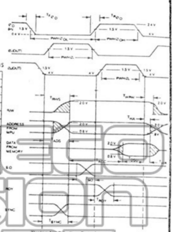
3) Also refer to 6507 and 6532 data specification.

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage Logic, $\emptyset_{2\,(in)}$	VIH	Vss + 2.4	—	Vcc	Vdc
Input High Voltage $\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, S.O.		Vss + 2.0	—	—	Vdc
Input Low Voltage Logic, $\emptyset_{2\,(in)}$	VIL	Vss − 0.3	—	Vss + 0.4	Vdc
$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, S.O.		—	—	Vss + 0.8	Vdc
Input Leakage Current (V_{in} = 0 to 5.25V, Vcc = 5.25V) Logic (Excl. RDY, S.O.)	Iin	—	—	2.5	μA
$\emptyset_{2\,(in)}$		—	—	10.0	μA
Three State (Off State) Input Current (V_{in} = 0.4 to 2.4V, Vcc = 5.25V) Data Lines	ITSI	—	—	10	μA
Output High Voltage (I_{OH} = −100μAdc, Vcc = 4.75V) SYNC, Data, A0-A15, R/W	VOH	Vss + 2.4	—	—	Vdc
Out Low Voltage (I_{OL} = 1.6mAdc, Vcc = 4.75V) SYNC, Data, A0-A15, R/W	VOL	—	—	Vss + 0.4	Vdc

TABLE 7A - I/O Specification

READ/WRITE TIMING (LOAD = 1TTL) Unit/ns

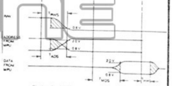
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX
Read/Write Setup Time from 6507	T_{RWS}	—	100	300
Address Setup Time from 6507	T_{ADS}	—	100	300
Memory Read Access Time	T_{ACC}	—	—	575
Data Stability Time Period	T_{DSU}	100	—	—
Data Hold Time—Read	T_{HR}	10	—	—
Data Hold Time—Write	T_{HW}	30	60	—
Data Setup Time from 6507	T_{MDS}	—	150	200
S.O. Setup Time	T_{SO}	100	—	—
SYNC Setup Time from 6507	T_{SYNC}	—	—	350
Address Hold Time	T_{HA}	30	60	—
R/W Hold Time	T_{HRW}	30	60	—
RDY Setup Time	T_{RDY}	100	—	—



Timing for Reading Data from Memory or Peripherals

CLOCK TIMING—6507 Unit/ns

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX
Cycle Time	T_{CYC}	1000	—	—
$Ø_{0(IN)}$ Pulse Width (measured at 1.5V)	$PWHØ_0$	460	—	520
$Ø_{0(IN)}$ Rise, Fall Time	$TRØ_0, TFØ_0$	—	—	10
Delay Time between Clocks (measured at 1.5V)	T_D	5	—	—
$Ø_{2(OUT)}$ Pulse Width (measured at 1.5V)	$PWHØ_2$	$PWHØ_{0L}-40$	—	$PWHØ_{0L}-10$
$Ø_{2(OUT)}$ Rise, Fall Time (measured .8v to 2.0v) (Load = 30pf + 1 TTL)	T_R, T_F	—	—	25



Timing for Writing Data to Memory or Peripherals

TABLE 7B - Timing Table

7.65 Hand Controller Connector J3 and J4

J3 Left Connector		J4 Right Connector	
Pin 1	PA4 I/O Table 7C	Pin 1	PA0 I/O Table 7C
Pin 2	PA5 I/O Table 7C	Pin 2	PA1 I/O Table 7C
Pin 3	PA6 I/O Table 7C	Pin 3	PA2 I/O Table 7C
Pin 4	PA7 I/O Table 7C	Pin 4	PA3 I/O Table 7C
Pin 5	Port A Input Item 8.32, Pin 10	Pin 5	Port C Input, Item Pin 35
Pin 6	Trg 1 Input Item 8.32, Pin 36	Pin 6	Trg 2 Input, Item Pin 35
Pin 7	+5V	Pin 7	+5V
Pin 8	-0.3V Negative bias	Pin 8	-0.3V negative bias
Pin 9	Port B Input, Item 8.32, Pin 39	Pin 9	Port D Input, Item 8.32, Pin 37

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage	V_{IH}	V_{SS} + 2.4	—	VCC	V
Input Low Voltage	V_{IL}	V_{SS} - .3	—	V_{SS} + .4	V
Input High Current, V_{IN} = 2.4V PA0-PA7, PB0-PB7	I_{IH}	- 100	- 300	—	µA
Input Low Current, V_{IN} = .4V PA0-PA7, PB0-PB7	I_{IL}	—	- 1.0	- 1.6	mA
Output High Voltage VCC = MIN. $I_{LOAD} \leq$ -100µA (PA0-PA7, PB0-PB7, D0-D7) $I_{LOAD} \leq$ -1mA (PB0-PB7)	V_{OH}	VSS + 2.4 VSS + 1.5	—	VCC	V
Output Low Voltage VCC = MIN. $I_{LOAD} \leq$ 1.6MA	V_{OL}	V_{SS}	—	VSS + .4	V
Output High Current (Sourcing) VOH ≥ 2.4V (PA0-PA7, PB0-PB7, D0-D7) ≥ 1.5V Available for other than TTL (Darlingtons) (PB0-PB7)	I_{OH}	- 100 - 3.0	- 1000 - 6.0	—	µA mA
Output Low Current (Sinking) VOL ≤ .4V (PA0-PA7) (PB0-PB7)	I_{OL}	1.6	—	—	mA

Table 7C, I/O Specification

7.7 System Performance Test Specification

Test cartridge number 92064 is used for following system performance test. Press game select switch advances each test.

7.71 Test #1: Color Adjust Screen

Power up, test cartridge inserted; set color, adjust potentiometer so that left side of screen is the same color as right side of screen. Initially right side of screen should be green. Deviation of left side green, relative to right side green may be determined from provided certified standards, which determine the extent left side of screen may safety deviate from right side of screen and still allow true color presentation.

The result of the data line and address line test is displayed in the region above and below the color bars. The left side indicates the result of the data line test. The right side indicates the result of the address line and RAM test, when both of the regions are green then the tests were both passed, when either one is red, this indicates a failure of that test. See figure 7.71A.

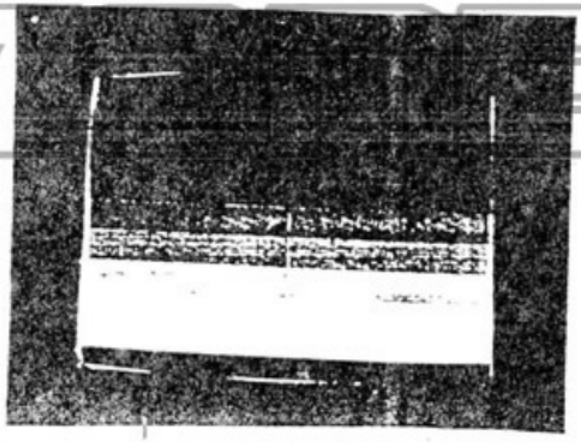


figure 7.71A
Color Adjust Screen

7.72 Test #2: Color Display Test

See Figure 7.72A.

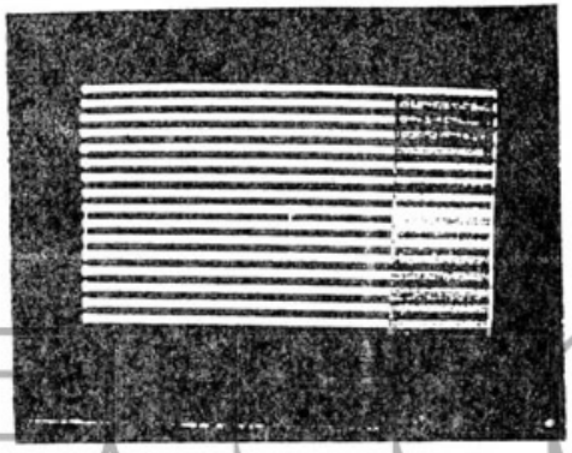


Figure 7.72A Color Display Screen

7.73 Test #3: Coincidence Test

Displays a series lines down the left side and 2 sets of 5 blue squares on the left and center of the screen. If the test is passed the top and bottom of the screen will be green, if the test fails, a large blue pair of stripes will appear where the failure took place and the top and bottom of the screen will be red. See figure 7.73A.

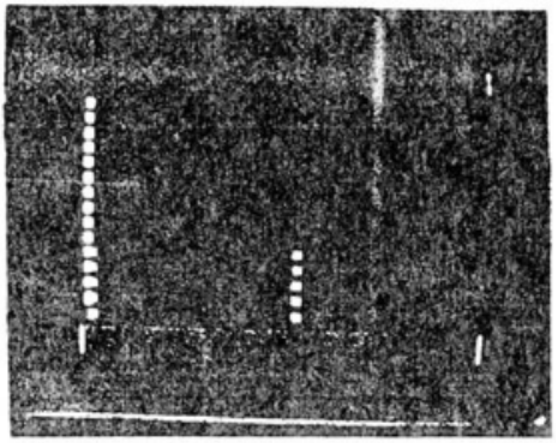


Figure 7.73A
Coincidence Test Screen

7.74A Test #4: Foreground Display Test

See figure 7.74A.

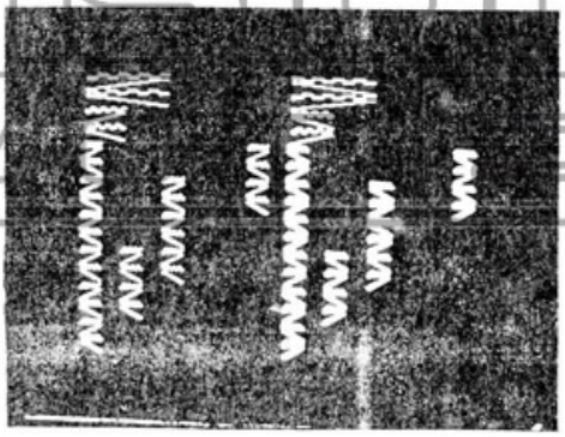


Figure 7.74A
Foreground Display Test

7.75 Test #5: Object Display Test

See Figure 7.75A

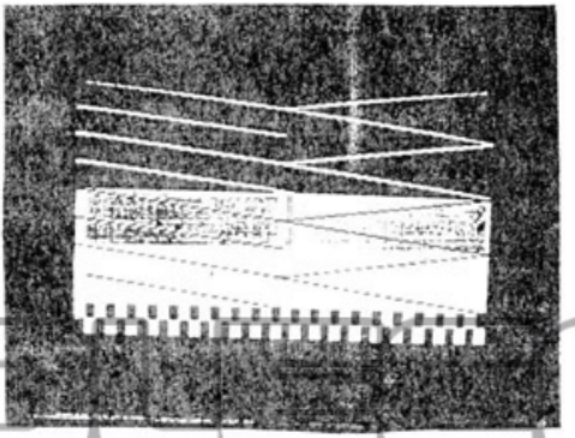


Figure 7.75A

Object Display Screen

7.76 Test #6: Projectile and Border Test

Also test Object Priority and Projectile Tracking.

See Figure 7.76A.

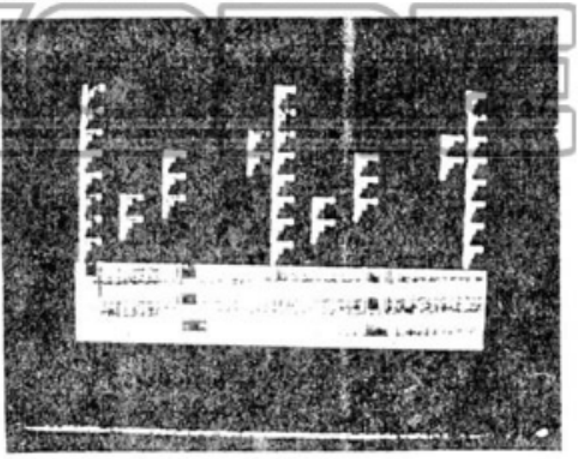


Figure 7.76A

Projectile and Border Test Screen

7.77 Test #7: Sound Test

An feedback circuit Figure 7.77A shall be installed to test sound output. A fail-screen 7.77B and pass-screen 7.77C shall be displayed.

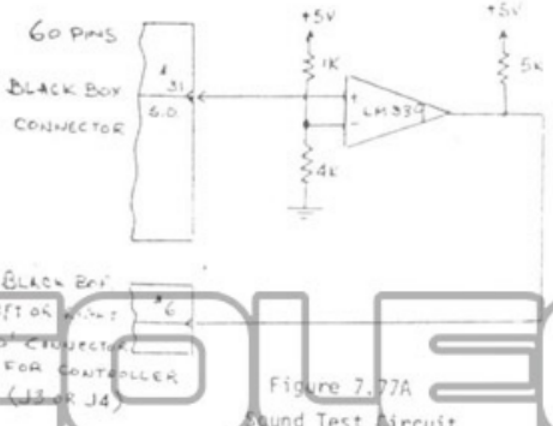
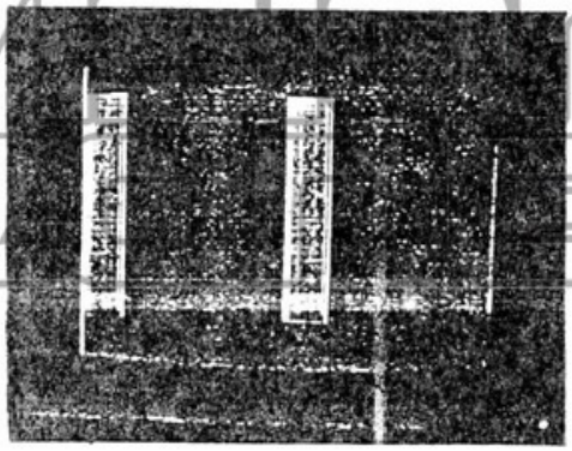
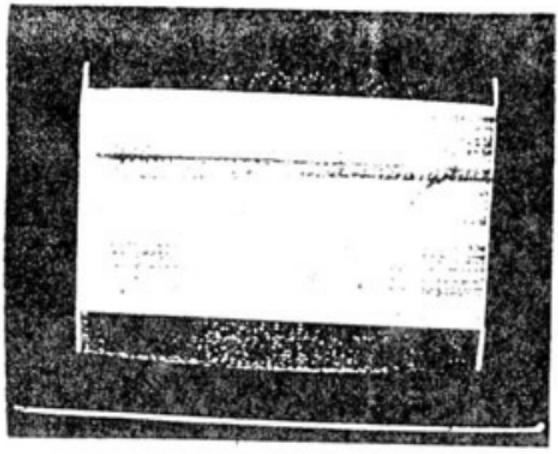


Figure 7.77A
Sound Test Circuit



7.77B Sound Test Fail Screen



7.77C Sound Test Pass Screen

7.78 Test #8: I/O and Switches Test

A test circuit, constructed per Figure 7.78A, shall be connected to the two 'D' connectors for controllers. After the connection of the test circuit, Figure 7.78B shall be displayed. After activation of Black-White/Color, two difficult slide switches and game reset push button switch, Figure 7.78C is displayed.

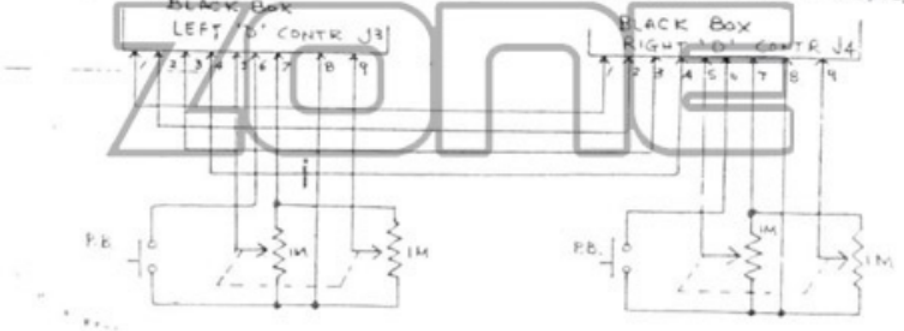


Figure 7.78A
Connector Test Circuit

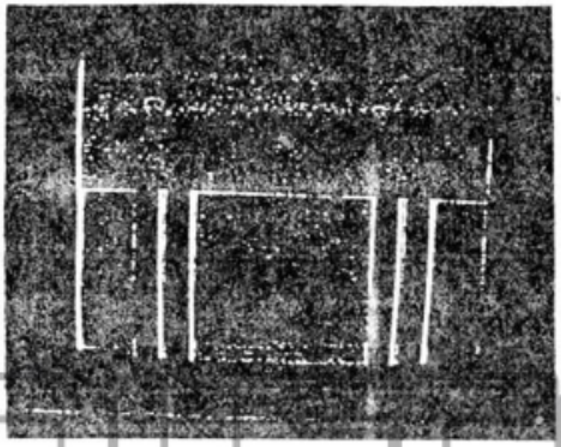


Figure 7.78B
I/O Test Screen

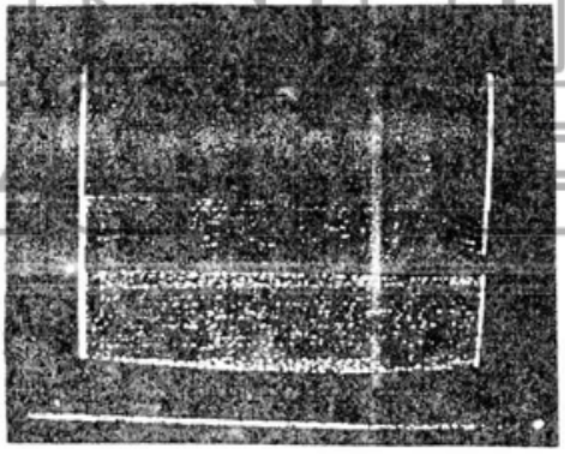


Figure 7.78C
I/O Test Screen Pass

Circuit 7.78A is also used in this test. Test screen 7.79A is displayed initially. Activation of two trigger buttons of circuit 7.78A should eliminate two vertical lines at each side. Turning the two potentiometers should moving the middle lines up or down.

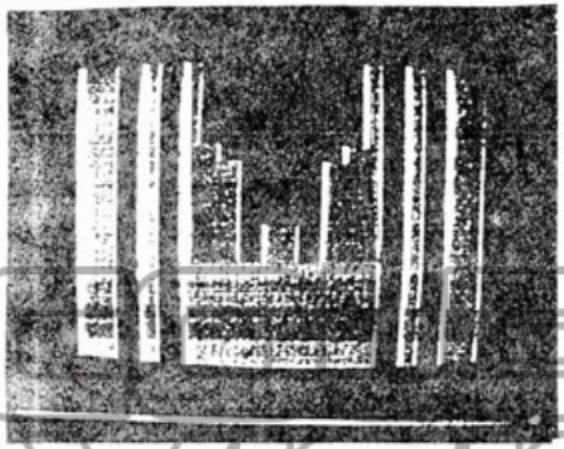


Figure 7.79
Pot and Trigger Test Screen

7.710 Test #10: Delayed Register Test

See figure 7.710A for display. A green top and bottom screen is displayed after passing all previous test. Red screen results when one or more previous tests fail.

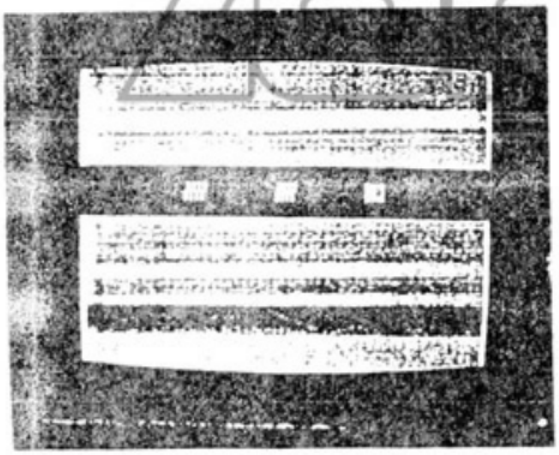


Figure 7.710A
Delayed Register Test

8. PRODUCT DESCRIPTION

The sole purpose of this expansion module is to provide interface between 'A' cartridges and ColecoVision console. Spring - return lid protects 24 pin female edge connector which is used for acception of 'A' cartridges. 60 pin female edge connector located at back side provides electrical and mechanical link between expansion module and ColecoVision console.

The Black box has two 9-pin male "D" connectors located at the front for connection of either ColecoVision or 'A' controllers.

Color-B/W slide switch is used to switch system to be compatible with black and white TV set. Two slide switches labeled LEFT DIFF. and RIGHT DIFF. are used to select difficulties levels for left and right controllers.

Momentary "SELECT" switch allows player to select games and "RESET" switch to reset/start games. In addition the ColecoVision console "RESET" switch specifically provides hardware reset to the Black Box.

8.1 Technical System Description

A PCB, fully shielded to FCC part 15 requirement, consist of three major systems, namely 6507 CPU System, 6532 - RAM - I/O - TIMER (RIOT) and custom video display generator 84002. System clock 3.58 MHZ is supplied by ColecoVision console via the edge connector.

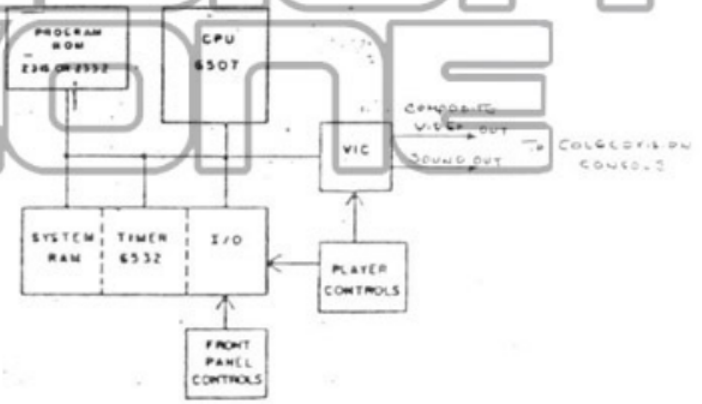


FIGURE 4

EXPANSION MODULE #1

The custom Video Interface Circuit (VIC) is an single N-Channel MOS LSI Integrated Circuit, which provides both analog and digital player inputs, Foreground, Moving Object, Projectiles, Border, and Audio Signals. The Microprocessor used in the system is the 6507. The ROMS used are the 2316 (16K) or 2332 (32K). The peripheral interfacing chip (PIC) is a 6532.

The game is Microprocessor controlled and each game definition is stored as a program in the ROM. The ROM contains the game rules, the score font, the object font, the background font or algorithm, and the sound algorithms. Each ROM can contain more than one game or variations of a game depending on game complexity.

The VIC develops Composite Video with Color Burst according to the NTSC video standard and uses a 3.579545 MHZ oscillator frequency supply by ColecoVision console. The display is non-interlaced. A block diagram of the system is shown in Figure 8A. The Microprocessor reads the stored program in the ROM and controls VIC to generate the video output. The VIC generates the Horizontal Sync, Horizontal Blanking, Color Burst, and Video Signals which contain the Color and Luminence signals. The Microprocessor keeps track of the number of horizontal lines scanned and controls the VIC to generate the Vertical Blanking and Sync. The VIC generates the sounds under control of the Microprocessor, which can control the frequency, shape, and amplitude.

The Microprocessor uses the PIC and VIC as the I/O interface for the player controllers (digital), player potentiometers (analog), and the front panel controls (digital). The system scratchpad RAM and Stack are in a 128 byte RAM in the PIC which also contains a programmable 8 bit timer.

The 128 byte RAM in the PIC is shared between the MPU stack and the system scratchpad RAM. The RAM is address transparent between $0080 thru $00FF and $0180 thru $01FF. This means that the same RAM appears in both of these address ranges simultaneously and care must be exercised not to let the stack alter the scratchpad RAM being used by the program.

8.2 SYSTEM MEMORY MAP

The following Memory Map outlines the System Memory for the Microcomputer System:

$F800-$FFFF	PROGRAM ROM HIGH (16K = 2K X 8)
$F000-$F7FF	PROGRAM ROM LOW (32K = 4K X 8)
$0280-$02FF	I/O INTERFACE & TIMER (PIC)
$0180-$01FF	STACK RAM (PAGE 1) (PIC)
$0080-$00FF	RAM (PAGE 0) (PIC)
$0000-$002C	VIC

8.3 E4002 VIC DESCRIPTION

The VIC is a Bus oriented device. The Microprocessor address and data busses enter the VIC and access the major functional areas. With the Address Bus the Microprocessor selects the area it desires to communicate with. The information is presented or received from the selected area on the Data Bus.

An external oscillator provides the 3.58 MHZ clock frequency for the VIC. The VIC then divides it by 3 to generate the clock for the Microprocessor.

The VIC internally generates the Horizontal Sync, Blanking, and Color Burst and generates 4 displayable colors per line (Object A/Projectile A, Object B/Projectile B, Border/Foreground, and Background). Each color is independently programmable, and each one has a priority over the other. Some of the priorities can be altered by the Microprocessor. There are 128 Programmable colors for each of the above.

There are two fully programmable Objects (Object A and Object B). Each of these Objects is 8 bits wide and is fully programmable which means that there are 255 visible combinations of display for each Object. There are two Object Font Registers for each Object. Each Object Font Register contains one Byte (8 bits) of data. The direction in which the data is scanned can be reversed. The horizontal size of the bits in the Object display can be programmed to be 1, 2, or 4 units wide. Each of the Objects can be programmed to be repeated one or two times after the original and at different intervals from the original Object.

There are two dedicated objects (Projectile A and Projectile B) that are related to the main Objects (Object A and Object B). These

Projectiles can only be 1, 2, 4, or 8 units wide. Projectile A can be programmed to track the horizontal movement of Object A. Projectile B can be programmed to track the horizontal movement of Object B. The Projectiles can be repeated horizontally in conjunction with the associated Object. Projectile A is repeated exactly as Object A and Projectile B is repeated exactly as Object B.

There is also a dedicated object (Border) that can be moved or used as a ball, Border, or center line. The Border can only be 1, 2, 4, or 8 units wide. The Border cannot be repeated.

The Foreground is a 20 bit memory that can be displayed in one of four methods horizontally. Each bit is 4 units wide and the active foreground area is 160 units wide. The foreground memory acts as a register. The register is 2-1/2 bytes of RAM (20 bits). The Foreground Register is displayed two times each line (40 bits/line).

An object can be made to appear over or under the Foreground and Border and can appear over or under another object based on a priority system. Object A, Object B, Projectile A, and Projectile B can be programmed as higher or lower priority than the Foreground and Border. Object A and Projectile A are always a higher priority than Object B and Projectile B.

The horizontal movement of each Object (A and B), Projectile (A and B), and the Border is controlled by the Microprocessor. Each of these 5 can be moved left or right relative to the Horizontal Reference Counter. Movement can be from -7 to +8 horizontal units per horizontal line sweep.

The VIC has a coincidence detection circuit that indicates when any two Objects, Projectiles, Foreground, Border, or any combination of

the above are coincidental with each other. A set of 15 comparators compares each object against the other and stores the result in a set of registers which can be read and reset by the Microprocessor.

The VIC has 4 analog inputs with Schmitt triggers for accurate repeat detection of the player potentiometer setting. The analog inputs use a resistor-capacitor circuit for the time constant; the resistor is a potentiometer that is controlled by the player. Each input has a programmable discharge transistor that can be turned on to discharge the capacitor in the RC timing circuit.

There are also 2 Trigger inputs which can be used as latching Input Ports. Whenever one of these inputs goes to a "0" level, this transition is stored in a latch that can be reset under software control. The latching mode is programmable and when turned off the data at the Trigger inputs is passed directly to the MPU when read.

The VIC contains two Sound generators each of the Sound generators are connected to one of the two Sound Output pins.

The Sound Generator consists of a Programmable Divider that divides the horizontal sweep frequency, a Sound Generator, and a programmable Output Driver. The Divider can be programmed to divide the 15.7 KHZ horizontal sweep frequency by 1 to 32. The Sound Circuit is programmable for 10 different sounds and tones. This circuit can produce a series of sounds from a simple tone to a complex random noise. The Output Driver can be programmed for 15 different output levels.

8.31 VIC GENERAL FEATURES

* 2 General Purpose Objects
* 3 Dedicated Objects
* Object Duplication (2 Programmable Repeat Objects)
* Object Size and Movement Under Microprocessor Control
* Programmable Object Priority
* 280 nsec Object Resolution
* Programmable Foreground
* Programmable Foreground Repeat or Mirroring
* 128 Programmable Colors
* Programmable Vertical Sync and Vetical Blanking Timing
* 2 Programmable Sound Generators
* 4 Analog Potentiometer Inputs
* 2 Digital Inputs (Edge Sensitive Programmable)
* 4 Displayable Colors per Horizontal Scan Line
* 4 Chip Select Lines for Address Decoding
* 40 Pin Dual-In-Line Package
* Page Zero Microprocessor Operation

8.32 The following is a summary of the input and output pins of the E4002 and their electrical characteristics for VCC/5.0V ±0.25V for TA/0-70°C.

Pin 1 Gnd.

Pin 2 Øo output push-pull output driver VOL/0.4V at 1.6mA VOH/-100.0uA at 2.4V signal is osc input divided by 3 and drives the Ø0 input of the 6507 (Pin 27).

Pin 3 RDY output drain output that pulls to GND VOL/0.4V at 1.6mA IOH/10.00uA at 5.25V. This pin drives RDY input (Pin 3) of 6507. Has a 4.7K pullup resistor (external) to VCC.

Pin 4 Sync output open drain output that pulls to GND VOL/0.4V at 1.6mA IOH/10.0uA at 5.25V. This pin is the horizontal and vertical sync output. Has a 3.3K pullup to VCC.

Pin 5, 6,7,8, and 9
LUM and blanking outputs same electrical parameters as pin 4. Pin 5 is LUM4, pin 6 is LUM2, pin 7 is LUM1, and pin 8 is BLNKG. Pin 9 color burst output same electrical parameters as pin 4 except a 1K pullup to VCC is used. This pin generates the color burst reference during horizontal blanking and the color burst during the active display lines.

Pin 10 Color adjust an input that is used to adjust the phase shift network for the color generator. This is a D.C. voltage. IIN/10.0uA max. VIN/0 to 6V.

Pin 11 Oscillator input. 3,579,545 HZ input. Input levels 0/0.4V 1/4.0V 50 pct duty cycle ±10%. Trise, Tfall less than 30N sec.

Pin 12, 13, 14, 15, 16, and 17

DB0 thru DB5 inputs VINL/0.4V VINH/2.4V IIN/10.0uA. These pins are connected to the 6507 DB0 thru DB5 outputs.

Pin 18, 19,

DB6, DB7 input/output pins. Tristate Outputs. Tristate input/10uA outputs on VOL/0.4V at 1.6mA, VOH/2.4V at 100uA.

Pin 20 VCC 5.25V to 4.75V 5.0V nom. ICC max 120.0mA.

Pin 21, 22, 23, and 24

Chip select inputs IIN/10.0uA.

Pin 25 R/W input IIN/10.0uA connected to 6507 R/W output (Pin 26).

Pin 26 Ø2 input IIN/10.0uA connected to 6507 Ø2 ouput (Pin 28).

Pin 27 and 28

Sound output pins connected together in system and connected together to a 1K pullup resistor to VCC. Each pin has 4 open drain output transistors binary weighted at 2.5K, 5.0K, 10.0K, and 20.0K plus or minus 20 pct with 1.0V VDS. Matching within 6 pct. IOH/10.0UA.

Pin 29, 30, 31, 32, 33, and 34

Address inputs AB thru AB5 connected to 6507 address lines. IIN/10.0UA.

Pin 35, 36

TGR1 and TGR2 inputs IIN/10.0US These inputs have Schmitt trigger inputs with approx 100 MV hysterisis min. and a trip point of approx 2.5V.

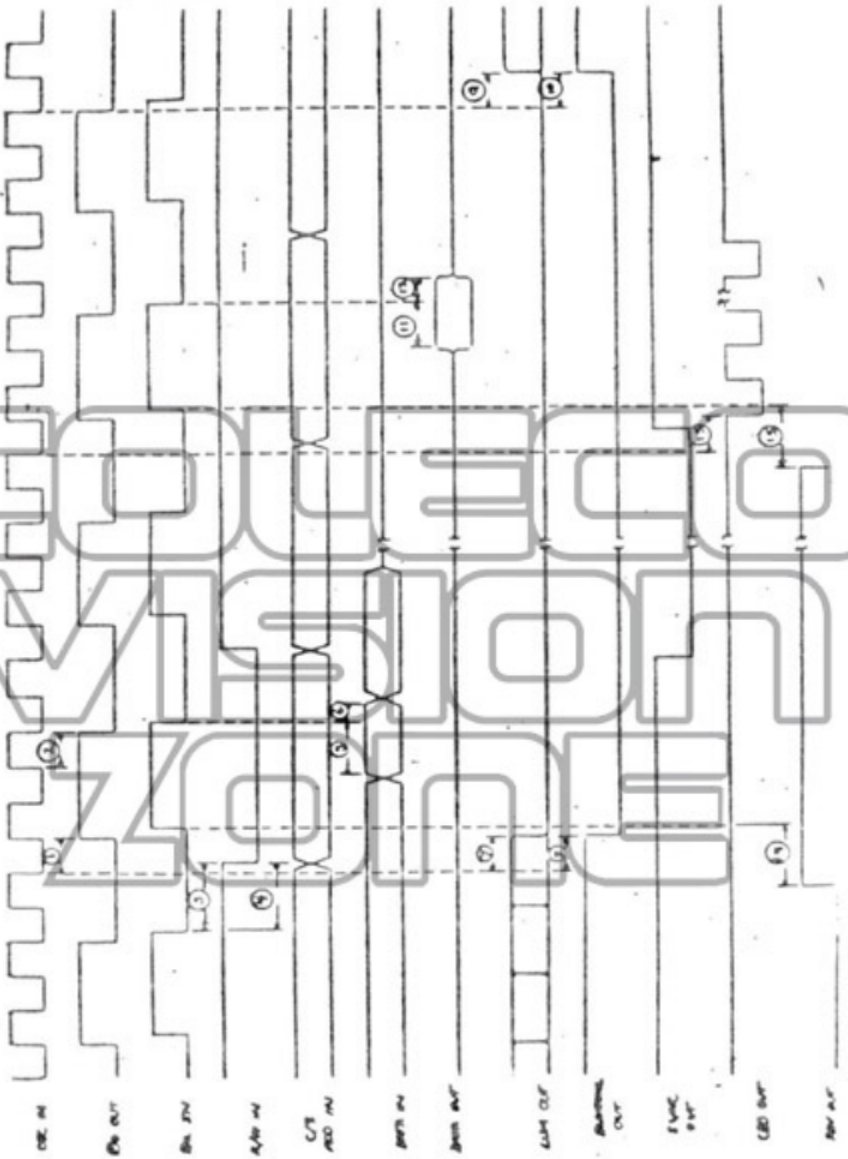
Pin 37, 38, 39, and 40

Potentiometer inputs same as pins 35 and 36 except for an open drain discharge transistor. IOL/250 US at 0.4V IOH/10.0 US.

8.33 E4002 TIMING SPECIFICATIONS

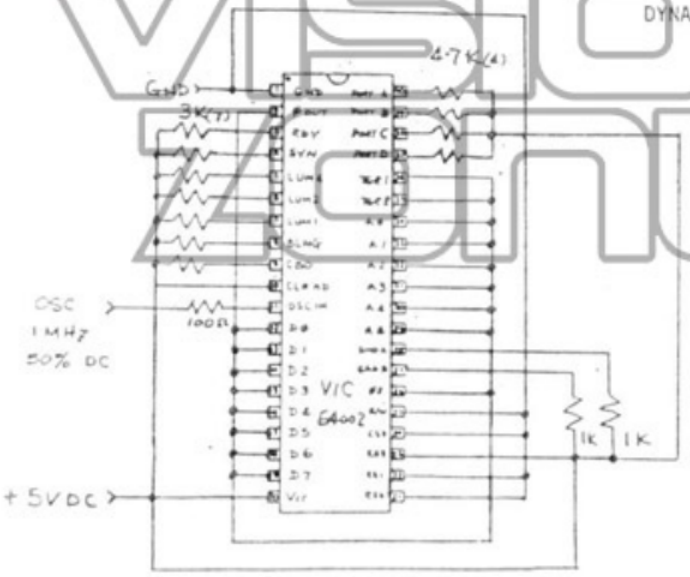
(1)	OSC IN to ϕ_0 OUT "1"	200 nsec
(2)	OSC IN to ϕ_0 OUT "0"	200 nsec
(3)	ϕ_2 IN to R/W	300 nsec
(4)	ϕ_2 IN to ADD & C/S IN	300 nsec
(5)	DATA IN to ϕ_2 IN DATA (DATA SET-UP)	200 nsec
(6)	ϕ_2 IN to DATA IN (DATA HOLD)	30 nsec
(7)	OSC IN to LUM OUT "0"	200 nsec
(8)	OSC IN to BLANKING OUT "0"	200 nsec
(9)	OSC IN to LUM OUT "1"	200 nsec
(10)	OSC IN to BLANKING OUT "1"	200 nsec
(11)	DATA OUT to ϕ_2 IN "0" (DATA SET-UP)	200 nsec
(12)	ϕ_2 IN to DATA OUT (DATA HOLD)	50 nsec
(13)	OSC IN to COLOR BURST OUT (REF)	200 nsec
(14)	RDY OUT "1" to ϕ_2 IN "1"	200 nsec
(15)	RDY OUT "0" to ϕ_2 IN "1"	200 nsec

E4002



E4002 PIN OUT

DYNAMIC BURN-IN CIRCUIT



COLECO INDUSTRIES	SPECIFICATION NUMBER 194	SHEET 35 OF 35	REV. B